

AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions and listings of claims in the above-referenced application:

- 1 1. (Original) An integrated circuit (IC) chip comprising:
2 a square-wave audio signal generator adapted to generate square-wave signals
3 at audio frequencies;
4 a counter adapted to digitally count from zero to a predetermined number;
5 a register adapted to hold a volume control value;
6 a comparator connected to said counter and connected to said register, said
7 comparator adapted to compare the count with the volume control value and produce a
8 modulation signal; and
9 an AND gate connected to said square-wave audio signal generator and
10 connected to said comparator, said AND gate adapted to combine, in a logical AND
11 operation, the audio frequency square-wave signal with the modulation signal.

- 1 2. (Original) The IC recited in claim 1 wherein said square-wave
2 audio signal generator generates a square-wave audio signal generator having a
3 frequency within a range from 500 Hz to five KHz.

- 1 3. (Original) The IC recited in claim 1 wherein said counter is a 5-bit
2 counter adapted to count from 0 to 31.

- 1 4. (Original) The IC recited in claim 1 wherein said counter operates
2 at a counter frequency on the order of MHz.

- 1 5. (Original) The IC recited in claim 1 wherein said register is a pulse
2 width register having five bits.

- 1 6. (Original) The IC recited in claim 1 wherein the integrated circuit
2 chip is an application specific integrated circuit chip (ASIC).

1 7. (Original) A method of generating modulated square-wave audio
2 signal, the method comprising:
3 generating a square-wave audio signal having a first audio frequency;
4 repeatedly counting a predetermined range of values generating count signals;
5 modulating the count signal with a volume control signal resulting in
6 modulation signal; and
7 modulating the square-wave audio signal with the modulation signal.

1 8. (Original) The method recited in claim 7 wherein the first audio
2 frequency is within a range from 500 Hz to five KHz.

1 9. (Original) The method recited in claim 7 wherein the digital
2 counting step counts from 0 to 31.

1 10. (Original) The method recited in claim 7 wherein the digital
2 counting step operates a counter frequency on the order of MHz.

1 11. (Original) The method recited in claim 7 wherein the volume
2 control signal is set at a value within a range counted by the digital counting step.

1 12. (Canceled)

1 13. (Currently amended) An apparatus comprising:
2 an integrated circuit (IC) chip adapted to generate a modulated audio
3 frequency square-wave signal;
4 an amplifier subsystem connected to said IC chip, the amplifier subsystem
5 adapted to filter the modulated square-wave audio signal and to amplify the filtered
6 audio signal, The apparatus recited in claim 12 wherein said IC chip comprises:
7 a square-wave audio signal generator adapted to generate square-wave signals
8 at audio frequencies;
9 a counter adapted to digitally count from zero to a predetermined number;
10 a register adapted to hold a volume control value;

11 a comparator connected to said counter and connected to said register, said
12 comparator adapted to compare the count with the volume control value and produce a
13 modulation signal; and

14 an AND gate connected to said square-wave audio signal generator and
15 connected to said comparator, said AND gate adapted to combine, in a logical AND
16 operation, the audio frequency square-wave signal with the modulation signal.

1 14. (Currently amended) The apparatus recited in claim 13 wherein
2 said square-wave audio signal generator generates a square-wave audio signal
3 ~~generator~~ having a frequency within a range from 500 Hz to five KHz.

1 15. (Original) The apparatus recited in claim 13 wherein said counter
2 is a 5-bit counter adapted to count from 0 to 31.

1 16. (Original) The apparatus recited in claim 13 wherein said counter
2 operates at a counter frequency on the order of MHz.

1 17. (Original) The apparatus recited in claim 13 wherein said register
2 is a pulse width register having five bits.

1 18. (Original) The apparatus recited in claim 13 wherein said amplifier
2 subsystem comprises a resistor-capacitor (RC) filter connected to a fixed gain
3 amplifier.